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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,710	07/08/2003	Thomas J. Ribarich	IR-2132 (2-3	9443
2352	7590	12/21/2004	EXAMINER	
OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403			ALEMU, EPHREM	
			ART UNIT	PAPER NUMBER
			2821	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/615,710

Applicant(s)

RIBARICH, THOMAS J.

Examiner

Ephrem Alemu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2004.
2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-14 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11-03-04.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Lesea (US 5,315,214).

Re claims 1-7, 11 and 12, Lesea discloses an integrated circuit for an electronic ballast control, comprising:

integrated circuit including half-bridge control circuitry (i.e., chip 50, 106, 300); ballast control circuitry; and power factor control circuitry for driving a power half-bridge (i.e., MOSFETs 52, 54, 112, 110) and operating a load (i.e. lamp) as claimed in claims 1-7 and 11-12 (Figs. 1-4; Col. 3, lines 7-45; Col. 4, lines 21-48; Col. 5, line 50- Col. 7, line 33).

Re claim 10, Wilhelm discloses a control circuit for controlling an electronic ballast for powering a lamp (Figs. 1-4), the control circuit having a plurality of states, comprising:

an undervoltage control state for disabling the electronic ballast; a preheat control state for switching a half-bridge in the electronic ballast at a first frequency and providing power factor correction with a fast response time; an ignition ramp control state for starting the lamp connected to the electronic ballast, with the half-bridge switching at a second frequency; a run control state with the power factor correction operating in low gain with optimized power factor

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correction; and a fault control state for protecting the electronic ballast based on a set of fault criteria (Figs. 1-4; Col. 3, lines 7-45; Col. 4, lines 21-48; Col. 5, line 50- Col. 7, line 33).

Re claims 8 and 9, given Lesea control circuit having a plurality of states as for controlling an electronic ballast as discussed in claim 10, the method for controlling an electronic ballast as claimed in claims 8 and 9 is inevitable (Figs. 1-4; Col. 3, lines 7-45; Col. 4, lines 21-48; Col. 5, line 50- Col. 7, line 33).

Re claim 14, Lesea discloses a single chip integrated ballast control (Fig. 2), comprising: a half bridge driver circuit and a control circuit (i.e., chip 50, 106, 300) for controlling and driving a half bridge switch (i.e., MOSFETs 52, 54, 112, 110) configuration (Figs. 1-4; Col. 4, line 49- Col. 5, line 8) ; and

a power factor correction circuit (i.e., chip 50, 106, 300) including power factor correction circuit) coupled to the control circuit (i.e., coupled within chip 50) and operable to control input power to improve a ballast power factor (Figs. 1-4; Col. 3, lines 7-45; Col. 4, lines 21-48; Col. 5, line 50- Col. 7, line 33).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ephrem Alemu whose telephone number is (571) 272-1818. The examiner can normally be reached on M-F Flex hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don K Wong can be reached on (571) 272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Grumbler

EA
12-08-04